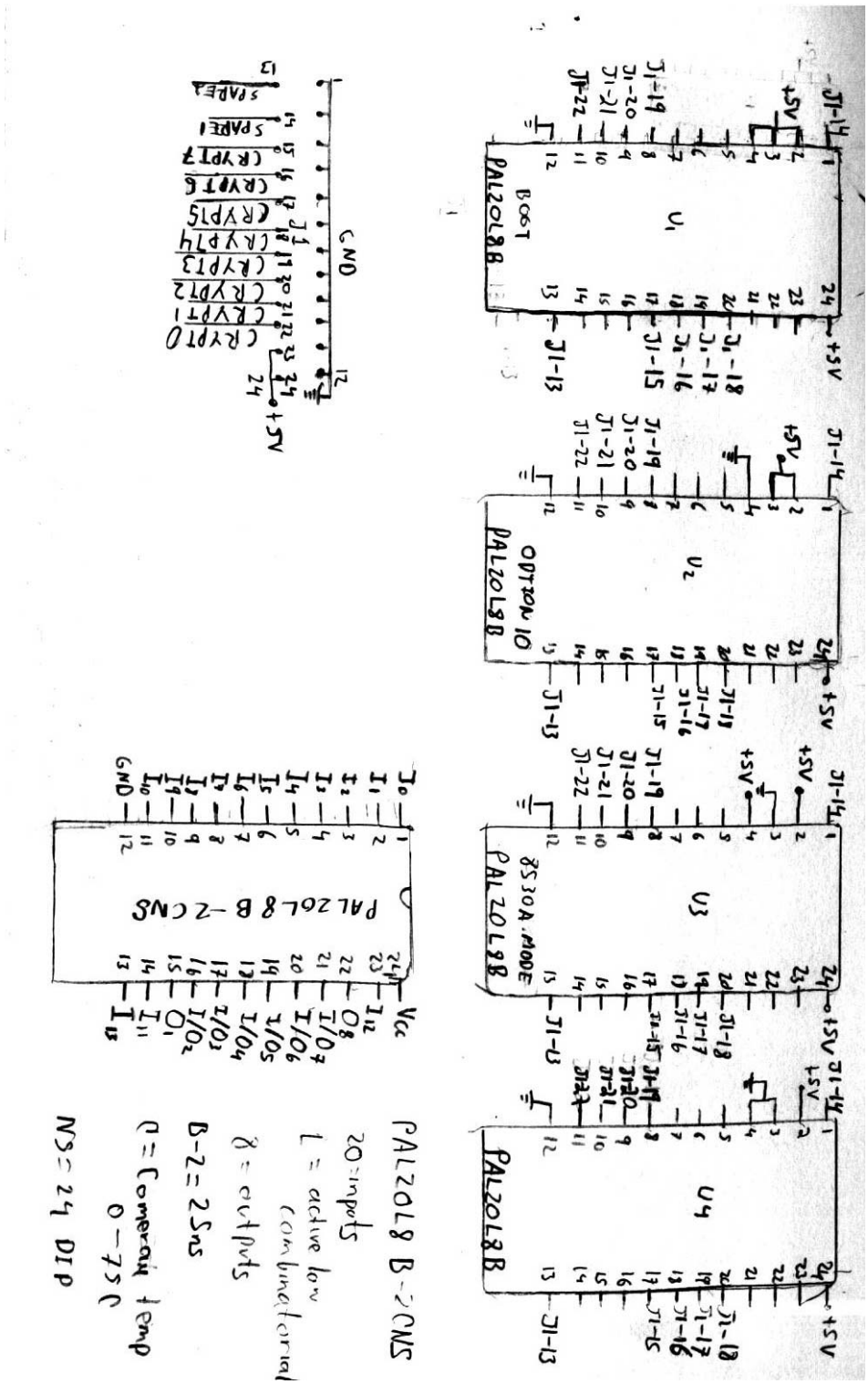
Introduction:

The 8510C went officially out of support on April 1st, so after more than 40 years of service one of the best analyzers of all times is finally obsolete. It is a shame that component level schematics are no-where-to-be-found according to some non-official reports. Nonetheless, for hobby and general RF work the 8510 seems to be a viable and affordable surplus-market alternative; furthermore it seems that the interest of "keeping it alive" will grow as time goes by.

We understand that the new generation of Agilent analyzers offer superb characteristics, performance and functions that 8510-trained engineers always dreamed of. Also, it is understandable that business sections of Agilent want to keep revenue as high as possible for the new models but not everybody can afford a new PNA analyzer with the frequency coverage of a good and complete 8510; specially: hobbyist, students, some universities and start-up companies. Things are a bit different when you are the owner of a system and cash is a bit on the low side; as an exercise, it would be interesting to ask to one of the development engineers of the PNA, to buy one and try to keep it running while paying everything out of your own pocket.

This document is the beginning of an effort to preserve the good old 8510 for hobby use and the memory of all the people who worked on the development of such great system. Just another example of the "old HP way" that people got to love so much; and to the memory of Bill and Dave who created one of the most amazing companies of all times.



Security Key Module Schematic

Security Key Module

One of the most frustrating situations occurs when any of the PAL (PAL20L8B-2CNS, Programmable Array Logic) modules in the security key assembly stops functioning properly. While we do not condone enabling options that were not purchased (because it tends to dilute the value of the rest of other 8510 systems), the following information should provide enough information to maintain a safe backup of the original module which is no longer available from Agilent.

The four PAL key generators perform the following functions:

- U1(boot key generator): the generated key allows the system to boot and every major firmware revision (for example going from 6.XX to 7.XX) needed a new one. Higher firmware revision PAL is backward compatible, meaning it will run with previous firmware versions; U1 PALs from previous revision will not work with higher revision firmware. The instrument will show “8510 Security Key not installed” or a similar message.
- U2: enables option 10 (Time domain measurements) very useful function for de-embedding and separating discontinuities.
- U3: enables 8530A personality Microwave Receiver for radar cross section and antenna measurements. Requires 8530A LIF disk software.
- U4: according to Agilent engineers it was never used.

The PAL modules are connected in parallel and share the same inputs from connector J1 (J1 pins 13,14,19,20,21,22; pins 13,1,8,9,10,11 on the PAL20L8 IC) and outputs (J1 pins 15,16,17,18; pins 17,18,19,20 on the PAL20L8 IC) and have some selection lines on pins 2,3 and 4 (PAL pinout).

The parallel connection suggests that there must be enable signals coming from the J1 connector that work in conjunction with the selection lines on pins 2, 3 and 4 of the PAL to enable/disable the output of each PAL IC. Otherwise, output will be shorted together.

The PAL20L8B-2CNS is a pure combinatorial module (there are no fip-flop or registers) but there is the possibility that some internal feedback from the output to the input was implemented. The attached datasheet describes the PAL20L8B-2CNS in detail.

Generation of a backup module would require the use of a logic analyzer and some or all of the following steps:

- Remove the PALs from the module and probe the pins to identify which pins are actual inputs.
- It will be necessary to identify output enable codes. Direct connection of pins 2, 3 and 4 on the PAL20L8 suggests that there must be at least two extra “output enable” lines.
- Once inputs are fully identified and combined with the rest of selection lines it will be necessary to check the outputs and identify the logic function being implemented.
- Step three would require connecting one PAL at a time, since connecting more than one would be a bit difficult to follow.
- Some logic analyzers are able to extract and generate the logic function while general PLD compilers can generate the required programming file for implementation in more modern programmable logic devices.

The above information is believed to be accurate for Rev. A of this document. Comments can be posted on the HP-Agilent yahoo newsgroup or sent to 8510c.project@gmail.com. If you believe this documents violates any IP, please send a relevant message and it will be removed.